REMARKS

Claims 1-5, 8-16 and 19-31 are pending in the present application.

Claims 1, 12, 23, 27 and 30 were amended herein.

Reconsideration of the claims is respectfully requested.

35 U.S.C. § 101, Statutory Subject Matter

Claims 1-5, 8-16 and 19-31 were rejected under 35 U.S.C. § 101 as being directed to non-statutory subject matter. This rejection is respectfully traversed.

The Office Action states:

> [C]laims 1-5, 8-16 and 19-31 merely disclose series mental [sic] steps/ components for adding two arguments without disclosing a practical/physical application. Further, the claims appear to preempt every substantial practical application of the idea embodied by the claim.

Paper No. 20080213, page 2. Independent claims 1, 12 and 23 each recite adder cells arranged in rows of adder cells, at least one of which includes first and second adder cells, and first and second pass gates. Claims 5 and 16 further recites a third adder within the row. Claims 11 and 22 each recite that the row contains N adder cells while a prior row contains fewer than N adder cells. Claim 12 additionally recites an instruction execution pipeline comprising N processing stages. Claims 24-25 and 28-29 each recite inverters. Claims 26-27 and 30-31 each recite multiplexers. By specifying operation of hardware components, the claims thus recite a practical application rather than a mere series of mental steps/components.

Nor do the claims preempt every substantial practical application of adding two M-bit components. For example, the a conditional carry-out bits $C_{X+1}(1)$ and $C_{X+1}(0)$ may be computed using logic gates in all instances (i.e., whether the operand bits are equal or not equal), rather

than being passed through by pass gates when the operand bits are not equal.

Therefore, the rejection of claims 1-5, 8-16 and 19-31 under 35 U.S.C. § 101 has been overcome.

35 U.S.C. § 102 (Anticipation)

Claims 1-5, 8-16 and 19-31 were rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 4,682,303 to *Uya*. This rejection is respectfully traversed.

A claim is anticipated only if each and every element is found, either expressly or inherently described, in a single prior art reference. The identical invention must be shown in as complete detail as is contained in the claim. MPEP § 2131 at p. 2100-67 (8th ed. rev. 6 September 2007).

Independent claims 1, 12 and 28 each recite that the second adder cell within a given row generates conditional carry-out bits $C_{X+1}(1)$ and $C_{X+1}(0)$ by propagating conditional carry-out bits $C_X(1)$ and $C_X(0)$ through first and second pass gates, respectively, when operand bits A_{X+1} and B_{X+1} are not equal. Such a feature is not found in the cited reference.

The Office Action asserts that NAND gate 54 and inverter 55 within the structure depicted in *Uya* satisfy the claim limitations of first and second pass gates. Paper No. 20080213, page 4. As an initial matter, Applicants note that the interpretation of "pass gates" advanced in the Office Action is not supported by any evidence of record, such that use of that interpretation is arbitrary and capricious. The Office Action states:

> [T]he claims do not define or address specifically what are the first and second pass gates respectively. Thus, as long as the cited reference discloses conditional carry-out bits are passing through logic gates, it would meet this claimed invention.

Paper No. 20080213, page 10. The Office Action thus interprets "pass gates" as encompassing any logic gate. This interpretation is not supported by any evidence of record and is inconsistent with usage of the term within the specification, and is therefore NOT "reasonable," such that reliance on the interpretation to reject the pending claims is arbitrary and capricious.

During prosecution, claims are given their broadest reasonable interpretation in light of the specification. MPEP § 2111, page 2100-37 (8th ed. rev. 6, September 2007). Under this mandate, claim terms are accorded their "plain meaning" – that is, the ordinary and customary meaning that the claim term would have to a person of ordinary skill in the art at the time of the invention – unless that plain meaning is inconsistent with the specification. MPEP § 2111.01(I) and (III), pages 2100-38 to 2100-40. However, the context in which the claim term is used in the specification should be considered in determining whether an interpretation accurately reflects the plain meaning of the claim term, together with evidence of customary usage by skilled artisans. MPEP § 2111.01(III), pages 2100-39 to 2100-40 ("It is the use of the words in the context of the written description and customarily by those skilled in the relevant art that accurately reflects both the 'ordinary' and the 'customary' meaning of the terms in the claims."). In particular, if more than one interpretation is possible based on "extrinsic" evidence (sources of support for an interpretation other than the specification), the specification must be consulted to determine which meaning is most consistent with applicant's use of the term(s). *Id.* at 2100-40. Only when more than one extrinsic definition is consistent with the use of the words in the specification can the claim terms be construed to encompass all such consistent meanings. *Id.*

Moreover, it is not sufficient to merely articulate a *conceivable* interpretation that might

be accorded to claim terms, since the proper interpretation is limited to broadest *reasonable* interpretation. Accordingly, the interpretation adopted must find support in the evidence ("intrinsic" or "extrinsic") of record. *Dickinson v. Zurko*, 527 U.S. 150, 164 (1999) (review of Patent Office record-based factual findings governed by arbitrary and capricious, substantial evidence standards of Administrative Procedure Act, 5 U.S.C. § 706(2)(A), (E)); *In re Morris*, 127 F.3d 1048, 1055 (Fed. Cir. 1997). An agency decision that is not based on a consideration of relevant facts and which is a clear error of judgment (i.e., one that lacks rationality) is arbitrary and capricious. *In re Gartside*, 203 F.3d 1305, 1312 (Fed. Cir. 2005). An agency decision that is not supported by more than a mere scintilla of relevant evidence, sufficient for a reasonable mind to accept as adequate to support the conclusion and not consisting solely of mere uncorroborated hearsay or rumor, is not supported by substantial evidence. *Id.*

In the present matter, the Office Action identifies no basis for the interpretation proposed for "pass gates." The interpretation suggested is contrary to the specification, drawings and claims of the present application (the "intrinsic" evidence), which in every instance use the term "pass gates" to refer to structures that are different from logic gates. For example, the specification and drawings use the term "pass gate" separately from "logic gate," and separately from specific logic gates such as inverters, NOT-AND (NAND) gates, NOT-OR (NOR) gates, exclusive-OR (XOR) gates and exclusive-NOR (XNOR) gates.

The Office Action neither asserts that the suggested interpretation of "pass gates" is based on any particular reference or other extrinsic evidence, nor identifies any evidence of record that "pass gates" is a particular term of art understood by those of ordinary skill to mean

any logic gate. In fact, those skilled in the relevant art understand that pass gates are different from logic gates, since a different symbol is employed to represent pass gates than are used to represent the various logic gates. To the extent that the Office Action purports to take official notice of alleged usage of the term "pass gates" to refer to any and all logic gates, Applicants respectfully traverse the official notice and request that evidence of such usage be made of record.

Because the suggested interpretation is not supported by any evidence of record (intrinsic or extrinsic), that interpretation is merely a conceivable interpretation, and not a reasonable interpretation supported by substantial evidence. In addition, to the extent that "pass gates" is actually used in the relevant art to refer to any and all logic gates, such a meaning is inconsistent with the usage of that term in the written description, where the term is employed solely to refer to controlled switches, structures that pass signal through unchanged. One skilled in the relevant art at the time the application was filed would therefore understand, in light of the specification and drawings, that the proper meaning of the term "pass gates" to most accurately read on switching structures that selectively pass signals through without inversion or other combination logic conditions, and NOT on any and all pass gates. Accordingly the Office Action's reliance on that interpretation in rejecting the pending claims is arbitrary and capricious.

To the extent that the Office Action relies on the fact that logic gates may be implemented using pass gates therein as part of an unstated assertion of inherency, such reliance is improper. To establish inherency, the evidence must make clear that the feature is necessarily present in the process or structure described in the reference; the fact that a certain result or

characteristic may occur or be present in the prior art is not sufficient to establish the inherency. MPEP § 2112(IV), page 2100-47. No evidence of record suggests that the logic gates 54 and 55 are implemented by pass gates.

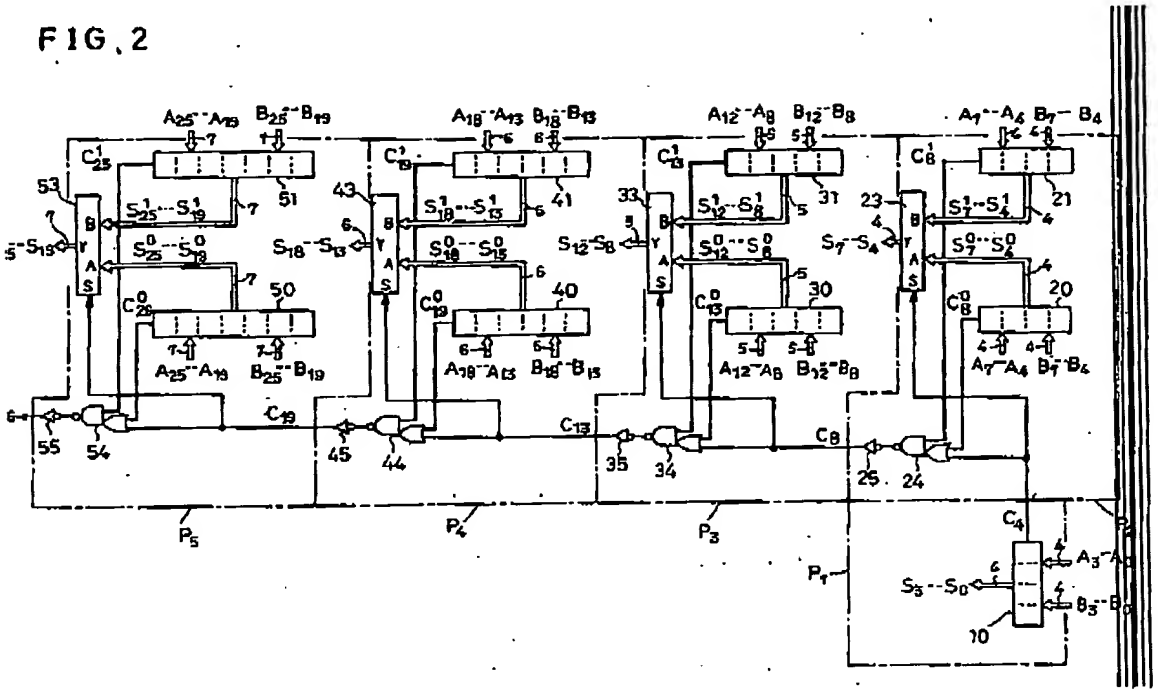
Regardless, independent claims 1, 12 and 28 each recite that the recited pass gates propagate conditional carry-out bits $C_X(1)$ and $C_X(0)$ as conditional carry-out bits $C_{X+1}(1)$ and $C_{X+1}(0)$, respectively, when operand bits A_{X+1} and B_{X+1} are not equal. The NAND gate 54 and the inverter 55 of *Uya* do not propagate received conditional carry bits C^0_{25} and C^1_{25}, but instead compute a logical combination of C_{19}, C^0_{25} and C^1_{25}.

Moreover, independent claims 1, 12 and 28 each recite that the recited pass gates propagate conditional carry-out bits $C_X(1)$ and $C_X(0)$ as conditional carry-out bits $C_{X+1}(1)$ and $C_{X+1}(0)$, respectively, when operand bits A_{X+1} and B_{X+1} are not equal. The cited portion of *Uya* contains no logic conditioning the operation of NAND gate 54 and inverter 55 on a determination that bits A_{25} and B_{25} are not equal. To the extent that the Office Action relies on an unstated assertion that unconditionally compute a logical combination of C_{19}, C^0_{25} and C^1_{25} (i.e., both when bits A_{25} and B_{25} are equal and when bits A_{25} and B_{25} are not equal), such an interpretation of the claims effectively reads the limitation "when operand bits A_{X+1} and B_{X+1} are not equal" completely out of the claims, giving that limitation no meaning whatsoever. Such an interpretation of the claims is arbitrary and capricious.

Finally, independent claims 1, 12 and 28 each recite that the second one of the adder cells within a particular row employ the recited pass gates to propagate conditional carry-out bits $C_X(1)$ and $C_X(0)$ as conditional carry-out bits $C_{X+1}(1)$ and $C_{X+1}(0)$, respectively, when operand

bits A_{X+1} and B_{X+1} are not equal. NAND gate 54 and inverter 55 are not part of an adder cell within adders 50 and 51:

FIG. 2



As conceded in the Office Action in connection with claims 11 and 22, adders 50 and 51 are rows of adder cells within block adder P_5 (where block adder P_5 contains one more adder cell than block adder P_4, block adder P_4 contains one more adder cell than block adder P_3, etc.). NAND gate 54 and inverter 55 are not part of the adder cells within adders 50 and 51 that operate on bits A_{25} and B_{25}, and accordingly those adder cells within adders 50 and 51 that operate on bits A_{25} and B_{25} cannot be said to constitute a second adder cells within one of a plurality of rows of adder cells that is operable to generate both conditional carry-out bits $C_{X+1}(1)$ and $C_{X+1}(0)$ by propagating conditional carry-out bits $C_X(1)$ and $C_X(0)$ through first and second pass gates, respectively, when data bits A_{X+1} and B_{X+1} are not equal.

Therefore, the rejection of claims 1-5, 8-16 and 19-31 under 35 U.S.C. § 102 has been overcome.

If any issues arise, or if the Examiner has any suggestions for expediting allowance of this Application, the Applicant respectfully invites the Examiner to contact the undersigned at the telephone number indicated below or at ***dvenglarik@munckcarter.com***.

The Commissioner is hereby authorized to charge any additional fees connected with this communication (including any extension of time fees) or credit any overpayment to Deposit Account No. 50-0208.

Respectfully submitted,

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